REMARKS

Claim Rejections 35 U.S.C. § 102 (e)

The Examiner has rejected claims 8, 10, 12, and 124-128 under 35 U.S.C. §102 (e) as being anticipated by Yu et al. (U.S. 6,271,563, of record).

Applicants respectfully disagree with the Examiner. Applicants have amended claim 8. An embodiment of Applicants' claimed invention as claimed in claim 8, as amended, is shown in Figure 3I.

Claim 8, as amended, of Applicants' claimed invention, claims a gate electrode, including: a gate layer (320) located over a substrate (300); thin first spacers (330) located adjacent to opposite sides of the gate layer; thick second spacers (340) located adjacent to the thin first spacers, the thick second spacers having vertical sidewalls, wherein the gate layer, the thin first spacers, and the thick second spacers have approximately the same height; and a conductive layer (360) located over the gate layer, the conductive layer extending laterally over the thin first spacers but not over sidewalls of the gate layer and not over the thick second spacers. See Figures 3A-3I.

In contrast, the gate electrode of Yu et al. has a gate layer (20) with a height greater than either the thin first spacers (19) or the thick second spacers (22). Furthermore, the gate electrode of Yu et al. does NOT have a conductive layer located over the gate layer (20). In addition, the gate electrode of Yu et al. has a gate layer (20) that extends laterally over both the thin first spacers (19) and the thick second spacers (22). See Figure 5.

Thus, Yu et al. fails to teach each and every element of Applicants' claimed invention, as claimed in claim 8, as amended. Consequently, Yu et al. does not anticipate Applicants' claimed invention, as claimed in claim 8, as amended.

Claims 10, 12, and 124-128 are dependent on claim 8, as amended. Thus, Yu et al. also fails to teach each and every element of Applicants' claimed invention, as claimed in claims 10, 12, and 124-128. Consequently, Yu et al. also does not anticipate Applicants' claimed invention, as claimed in claims 10, 12, and 124-128.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections under 35 U.S.C. §102 (e) to claims 8, 10-12, and 124-128.

Claim Rejections 35 U.S.C. § 102 (b)

The Examiner has rejected claims 8, 10-12, 14, and 124-125 under 35 U.S.C. §102 (b) as being anticipated by Orlowski et al. (U.S. 5,741,736).

Applicants respectfully disagree with the Examiner. Applicants have amended claim 8. An embodiment of Applicants' claimed invention as claimed in claim 8, as amended, is shown in Figure 3I.

Claim 8, as amended, of Applicants' claimed invention, claims a gate electrode, including: a gate layer (320) located over a substrate (300); thin first spacers (330) located adjacent to opposite sides of the gate layer; thick second spacers (340) located adjacent to the thin first spacers, the thick second spacers having vertical sidewalls, wherein the gate layer, the thin first spacers, and the thick second spacers have approximately the same height; and a conductive layer (360) located over the gate layer, the conductive layer extending laterally over the thin first spacers but not over sidewalls of the gate layer and not over the thick second spacers. See Figures 3A-3I.

In contrast, the gate electrode of Orlowski et al. has a conductive layer (140) that extends laterally over the gate layer (34), the thin first spacers (19), and the thick second spacers (22). See Figure 14.

Thus, Orlowsky et al. fails to teach each and every element of Applicants' claimed invention, as claimed in claim 8, as amended. Consequently, Orlowski et al. does not anticipate Applicants' claimed invention as claimed in claim 8, as amended.

Claims 10, 12, 14, and 124-125 are dependent on claim 8, as amended. Thus, Orlowski et al. also fails to teach each and every element of Applicants' claimed invention, as claimed in claims 10, 12, 14, and 124-125. Consequently, Orlowski et al. also does not anticipate Applicants' claimed invention, as claimed in claims 10, 12, 14, and 124-125.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections under 35 U.S.C. §102 (e) to claims 8, 10, 12, 14, and 124-125.

Claim Rejections 35 U.S.C. § 103 (a)

The Examiner has rejected claim 123 under 35 U.S.C. §103 (a) as being unpatentable over Yu et al. (U.S. 6,271,563, of record) in view of Matsumoto et al. (U.S. 5,726,479, of record).

Applicants respectfully disagree with the Examiner. Claim 123 is dependent on claim 8. Applicants have amended claim 8. An embodiment of Applicants' claimed invention as claimed in claim 8, as amended, is shown in Figure 3I.

Claim 8, as amended, of Applicants' claimed invention, claims a gate electrode, including: a gate layer (320) located over a substrate (300); thin first

spacers (330) located adjacent to opposite sides of the gate layer; thick second spacers (340) located adjacent to the thin first spacers, the thick second spacers having vertical sidewalls, wherein the gate layer, the thin first spacers, and the thick second spacers have approximately the same height; and a conductive layer (360) located over the gate layer, the conductive layer extending laterally over the thin first spacers but not over sidewalls of the gate layer and not over the thick second spacers. See Figures 3A-3I.

In contrast, the gate electrode of Yu et al. has a gate layer (20) with a height greater than either the thin first spacers (19) or the thick second spacers (22). Furthermore, the gate electrode of Yu et al. does NOT have a conductive layer located over the gate layer (20). In addition, the gate electrode of Yu et al. has a gate layer (20) that extends laterally over both the thin first spacers (19) and the thick second spacers (22). See Figure 5.

Yu et al. does not teach thick second spacers that comprise silicon nitride, but, in the opinion of the Examiner, Matsumoto et al. does teach thick second spacers (7a, 7b) that comprise silicon nitride. See Figure 1. Also, see col. 10, lines 28-29.

However, combination of the gate electrode of Yu et al. and the thick second spacers comprising silicon nitride of Matsumoto et al. will still not produce the gate electrode of Applicants' claimed invention, as claimed in claim 123.

Consequently, Applicants submit that the two references cited by the Examiner do not teach, suggest, or render obvious Applicants' claimed invention, as claimed in claim 123.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections under 35 U.S.C. §103 (a) to claim 123.

CONCLUSION

Applicants believe that all claims pending, including claims 8, 10-12, 14, and 123-128, are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charge or fee, including a Request for Continued Examination, an extension of time fee, or other fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 50-0221.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: April 14, 2006

George Chen
Reg. No. 50,807

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

CERTIFICATE OF TRANSMISSION
(37 C.F.R. § 1.8(a))

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